# The Role of Wafer Foundries in Next Generation Packaging

David McCann, VP Packaging R+D
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### Solutions are Increasingly Silicon-Based

- RF moves from QFN to wICSP
  - Driven by footprint and cost



- Memory moves much closer to the logic in 2.5D and 3D
  - Driven by power reduction and increased bandwidth
- 3D memory stacks replace 2D DIMMs
  - Driven by bandwidth, density, footprint

Courtesy: Micron Technology

- Interconnect density increases
  - Driven by progressively denser Si nodes
  - Driven by SoC disaggregation







### Disaggregation

- SOC scaling is not delivering full entitlement of cost/area improvement
- Enables SoC "fission" into best cost-performance fit node for each chip
- Enables high bandwidth and increased performance per joule
- Enables re-use without re-design...lower risk and lower cost



But requires more complex packaging solutions

# **Reliability in New Packaging Technologies**



# New Supply Chain Model: Collaboration



- Collaboration by the experts in each field
- Development of solutions in one location with partners, aligned to customers preferred supply chain
- Early development to support BEoL definition
- Aligned Design Rules, PDK, Systems
- Partners fan-out technologies to their factories for smooth production ramp

# **Supply Chain Inter-Dependencies**

### **3D**

#### ✓ Impact of Packaging on TSVs and Transistors

✓ Impact of Thinning

Design Rules for Supply Chain Yield

✓ Definition of Yield Loss Ownership



2.5D

**√** Interposer Supply

Design Rules for Supply Chain Yield

Metallurgy and Process Decisions

✓ Definition of Yield Loss Ownership



# CuPillar

✓ Impact of Packaging on BEoL stack

√ Stress of CuP on ELK

Design Rules that Work for Packaging

Test Chips for Supply Chain





# **Drive Adoption by Driving Yield which Drives Cost**





### Technology Development Center at Fab 8 Ground Break April, 2013





### **Collaborative Development at TDC for Solutions**







# Thank You

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